Design of Low power multiplexers using different Logics

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1. Abstract:
Low power and high speed digital circuits are basic needs for any of digital circuit, Multiplexer is a basic circuit for any digital circuit. In this paper, different techniques of multiplexer designs like low risk Conventional technique, transmission gate, pseudo logic, NMOS pass transistor logic, Pass transistor logic techniques has been introduced and their comparison on the basis of power, delay and Area(number of transistor) is done. A low power Multiplexer has been introduced which consumes least power as compare to above mentioned logic but have more delay as compare to other ,On the basis of these analyses it is concluded that proposed multiplexer is better technique for designing an low power low area Multiplexer design but it has high delay as compare to other Multiplexer.

2. Keywords:
Multiplexer, Low power, Tanner, Transmission Gate technique

3. Introduction:
The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles [2].

This paper analyzes 2-to-1 multiplexer using complementary CMOS, and CMOS transmission gate, pseudo logic, NMOS pass transistor logic, Pass transistor logic styles. These implementations are compared based on the basis of transistor count, power dissipation, and delay.

A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output that is why it is also called a data selector. Multiplexer can also be used to implement any combinational circuit. So by simplifying design of multiplexer, design of many combinational circuits can be simplified [5]. Fig.1.1 and fig.1.2 show the block diagram and truth table for 2to1 multiplexer given below [5].

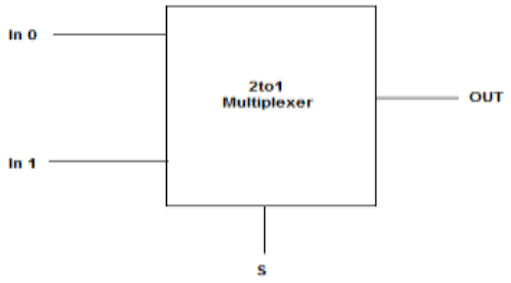

Fig.1.1 Block diagram of 2to1 multiplexer

S	OUT
0	In 0
1	In 1

Fig.1.2 Truth table for 2to1 multiplexer

The expression for 2to1 mux. is given below

$$OUT = \bar{S} I_{n0} + S I_{n1}$$

4. Different Logic Styles:

A logic style is the way how a logic function is implemented using a set of transistors. Various characteristics like speed, size, power dissipation and wiring complexity depend on a logic style and may vary considerably from one logic style to another and thus choice of proper logic style is very important for circuit performance. This paper shows two logic styles like Complementary MOS and Transmission gate.

4.1 Complementary MOS Logic Style

One of the most popular logic styles available today is the Complementary MOS. In this logic style, both N-type and P-type transistors are used to realize logic functions. The same signal which turns on a transistor of one type is used to turn off a transistor of the other type. This allows the design of logic devices using only simple switches, without the need for a pull-up resistor [3]. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull down network between the output and the lower voltage power supply rail and the collection of p-type MOSFETs in a pull-up network between the output and the higher voltage rail. Thus, if both p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be on when the n-type MOSFET is off, and vice-versa. A 2to1 multiplexer can be implemented using 12 transistors by this logic style. Fig.1.3 shows 2to1 multiplexer using CMOS logic style [7].

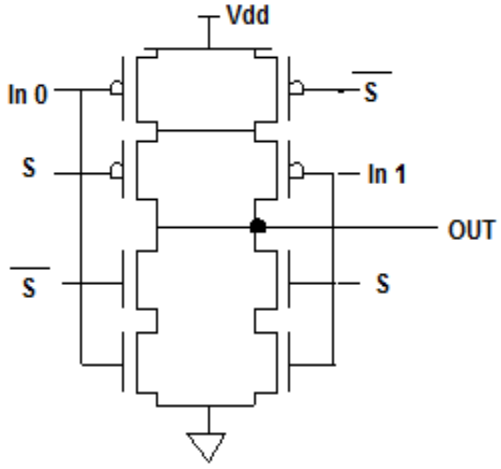

Fig.1.3 2to1 inverted multiplexer using CMOS

4.2 Transmission gate(TG) Logic Style

In this logic style N and P devices with sources and drains connected in parallel.V_g is the control signal for the N device, V_{gc} (complement of V_g) is the control signal for the P device. So When V_g is high (at V_{dd}) and V_{gc} is therefore low (at Gnd), the NFET and PFET are both ON[4]. (Depending upon

the devices' source potentials, one may be ON more strongly than the other.) The switch is therefore CLOSED and V_{out} will be the same logic level as V_{in}. When V_g is low (at Gnd) and V_{gc} is high (at V_{dd}), both devices are OFF. The switch is therefore OPEN and V_{out} will be independent of V_{in}. A 2to1 multiplexer can be implemented using 6 transistors by this logic style. Fig.1.4 shows 2to1 multiplexer using transmission gate logic style[1].

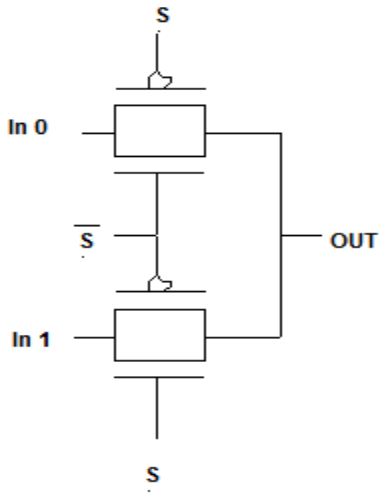

Fig.1.4 2to1 multiplexer using TG

4.3 Pass-transistor Logic style

The pass-transistor logic reduces the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source drain terminals. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation [7, 8].

Several pass-transistor logic styles such as NMOS Pass Transistor Logic, CMOS Transmission gate, and pass transistor logic(PTL) are considered to implement 2-to-1multiplexer[3,5,6].

Among all these NMOS Multiplexer is optimal. It uses two NMOS transistors and these two-pass transistors at the input select which signal to propagate. The logic levels will be deteriorated by the pass transistor. The threshold voltage of both pass-transistors should be identical for accurate operation. Figures in the simulation section represent design of 2-to-1 multiplexer using several logic styles.

5. Simulations

In this paper different logic styles styles CMOS, transmission gate, pseudo logic, NMOS pass transistor logic, Pass transistor logic were used to design 2to1 multiplexer. These multiplexers were designed on S-edit of Tanner tool on 45nm technology and simulated on T-edit with 1v power supply. Figures shows schematics of multiplexers designed using two logic styles.

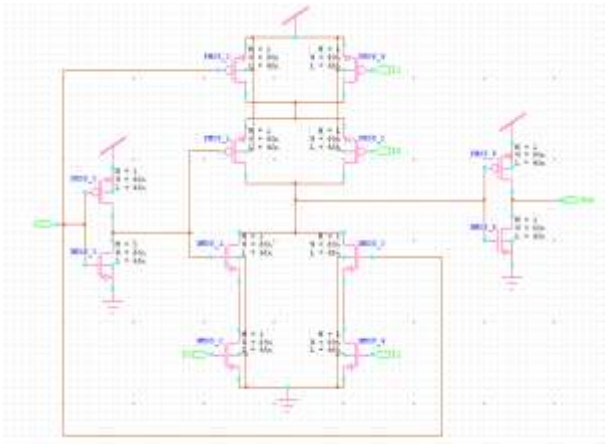

Fig.5.1 Schematic of CMOS multiplexer on tanner tool

And their simulation result is as shown in figure

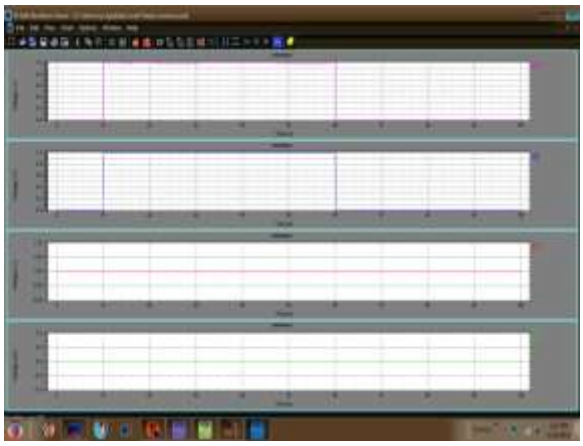

Fig.2.2 Simulation result of Conventional Mux.

And the Schematic of Transmission Gate 2:1 Mux. is given as

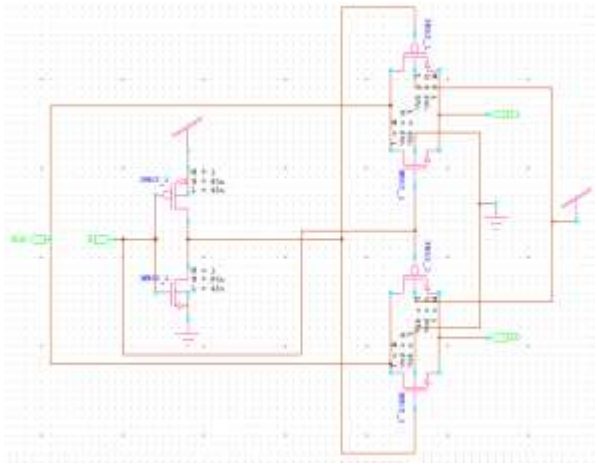

Fig.2.3 Schematic of TG multiplexer on tanner tool

And their Simulation result is given as

Fig2.4 Simulation result of Transmission gate Mux

And Schematic of Pseudo logic 2:1 Mux is

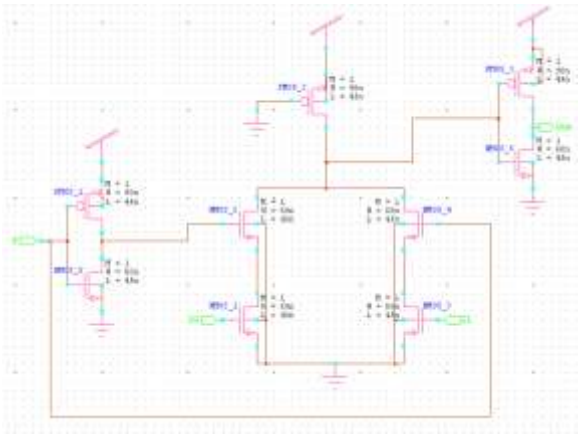

Fig2.5 Schematic of Pseudo logic multiplexer on tanner tool

And their simulation result is as shown in figure

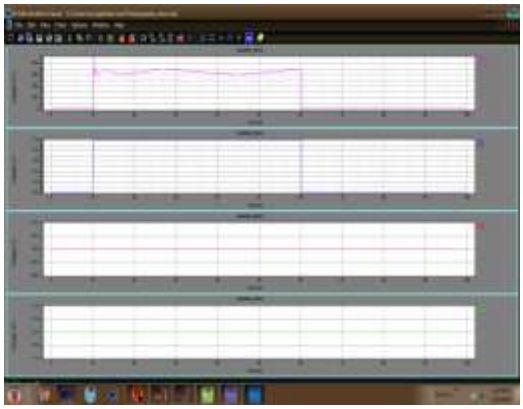

Fig2.6 Simulation result of Pseudo logic based 2:1 Mux

Now the Schematic result of NMOS pass transistor logic is as shown in figure

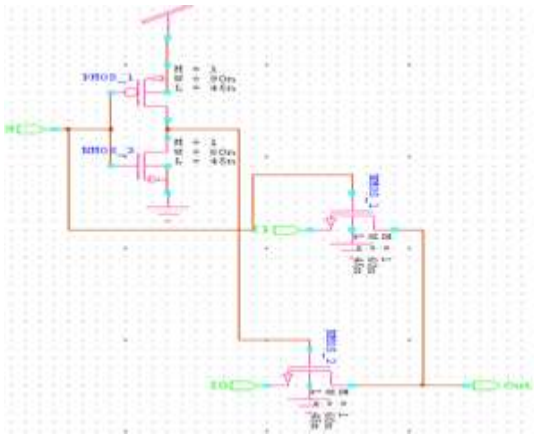

Fig2.7 Schematic of multiplexer NMOS logic on tanner tool

And their simulation result is as shown in figure

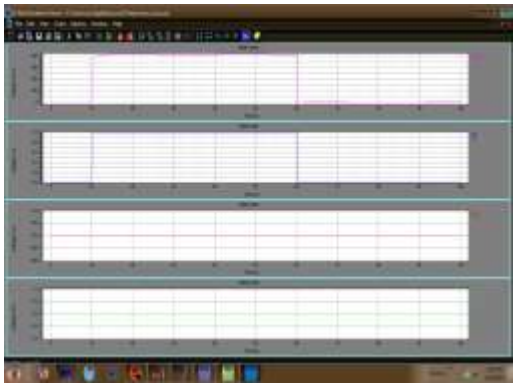

Fig2.8 Simulation result of NMOS logic Mux

And the Schematic figure of pass transistor logic using S-edit is as shown in figure

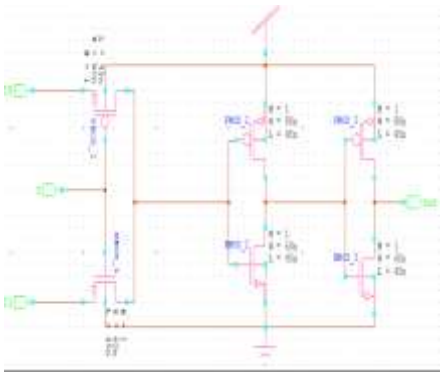

Fig2.9 Schematic of multiplexer pass transistor logic on tanner tool

And their Simulation result is as shown

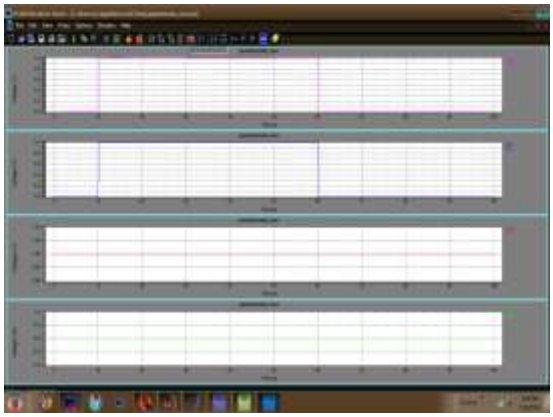

Fig2.10 Simulation result of pass transistor logic Mux

6. Proposed Low Power 2:1 MUX

In proposed technique we use a PMOS transistor at the bottom end which is in on condition when the output at th high level else it will be in off condition, when the bottom transistor is in off condition whole of PDN network have no use i.e. either it is on or off thus it save power and this type of transistors is known as sleep transistor

Schematic view of low power 2:1 Mux is as shown in figure

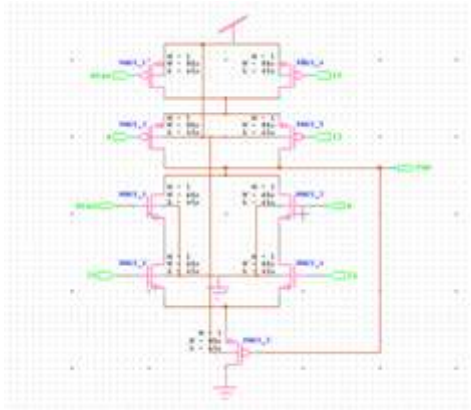

Fig3.1 Schematic of proposed multiplexer on tanner tool

And their Simulation result is as shown in figure

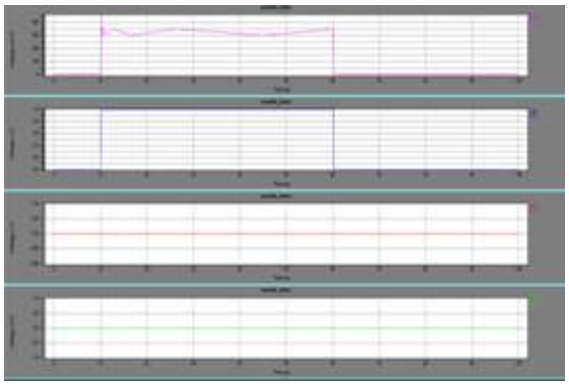

Fig3.2 Simulation result of proposed Mux

7. Experimental Results

Logic Style	No. of transistor	Power	Delay
CMOS	12	$2.388x10^{-7}$	$2.79x10^{-11}$
Transmission gate	6	$3.64x10^{-8}$	$5.26x10-^{12}$
pseudo logic	9	$2.26x10-^{8}$	$4.41×10-^{12}$
NMOS logic	4	1.41×10-8	$7.17×10-^{12}$
Pass transistor logic	6	1.57×10-8	$6.94×10-^{12}$
Proposed Design	13	1.01×10-8	$5.51×10-^{12}$

8. Conclusion

From the work carried out in this paper for implementation of 2 to 1 Multiplexer, we conclude that use of proposed logic style for implementation of 2 to 1 multiplexer provides improvement in power consumption, delay and transistor count when compared with implementation with CMOS logic style.

9. References

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